Printed Pages:02 **Sub Code: REC-301**

Paper Id: 233499 **Roll No.** | | | | | | | | | | |

B. TECH
(SEM-III) THEORY EXAMINATION 2022-23
DIGITAL LOGIC DESIGN

Time: 3 Hours ***Total Marks: 70***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 7 = 14**

(a) Draw a full adder using two half adders
(b) What is Modulus of a counter?
(c) What is the difference between Synchronous and Asynchronous sequential circuits
(d) What do you mean by race around condition in JK Flip Flop?
(e) What is the difference between Multiplexer and Encoder
(f) Write the canonical form of Y = (A+D)(B+C)(C+D)
(g) Convert $(554.423)_{10}$ to an Hexadecimal number

SECTION B

2. Attempt any *three* of the following: **7 x 3 = 21**

(a) Draw the basic circuit of the RTL NOR gate. Explain the operation.
(b) Implement the function F = ∑m(0,1,3,4,7,8,9,11,14,15) using 8:1 mux.
(c) Draw and explain 2-bit magnitude comparator.
(d) Using Quine McCluskey method, determine the minimal SOP expression for the following using decimal notation f=Σ m(1,4,7,9,12,14)+Σ d(2,13)
(e) Draw and explain the SISO, PISO right shift register.

SECTION C

3. Attempt any *one* part of the following: **7 x 1 = 7**

(a) Write the compressed truth table for a 4 to 2 line priority encoder with a valid output and simplify the same using K-Map. Design the logic circuit for the same.
(b) Design a combinational logic circuit to check for odd parity of three bits.

4. Attempt any *one* part of the following: **7 x 1 = 7**

(a) What is race around condition? How can it be avoided?
(b) Convert the decimal number 246.8 to base 3, base 5 and base 7.

5. Attempt any *one* part of the following: 7 x 1 = 7

(a) Design a BCD counter with D flip flops.

(b) Draw JK flip flop & write its Excitation table and characteristic equation.

6. Attempt any *one* part of the following: 7 x 1 = 7

(a) Design a 3-bit Up/Down ripple counter.

(b) An asynchronous sequential logic circuit is described by the following excitation and output function

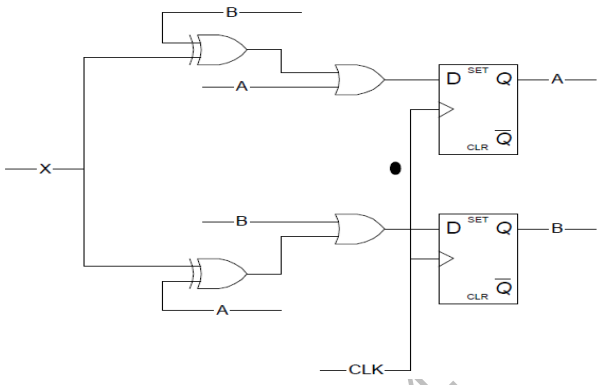
$$y= X_1X_2+(X_1+X_2)Y$$

$$Z=y$$

Draw the logic diagram of the circuit, Also derive the transition table and output map.

7. Attempt any *one* part of the following: 7 x 1 = 7

(a) Derive the state table and state diagram of the synchronous sequential circuit shown below (X is an input to the circuit). Explain the circuit function.



(b) Simplify following logic function using K-Map and realize using NOR gates.

$$f(w,x,y,z) = \pi M(1,2,3,7,10,11)+d(0,15)$$